PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s):	Mark G. Johnson, et al.		
Title:	Integrated Circuit Incorporating Three-Dimensional Memory Array with Dual Opposing Decoder Arrangement		
Application No.:	10/774,818	Filed:	February 9, 2004
Examiner:	Thong Quoc Le	Group Art Unit:	2827
Atty. Docket No.:	023-0025	Confirmation No.:	9232

August 25, 2006

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RESPONSE AFTER FINAL REJECTION (37 C.F.R. § 1.116)

This paper is being submitted following the Final Rejection mailed on May 25, 2006. In light of the Remarks herein, further consideration is requested.

No fee is believed due with this response. However, the Office is authorized to charge Deposit Account 50-0631 for any fee determined to be required by this paper.